Overview

1.1 Features

This LSI chip includes a high-speed image signal processor (ISP) for use with cameras, an AI accelerator, and a hardware engine which is capable of the real-time analysis of video data. This processor realizes processing from high-level sensing through to analysis, assessment, and execution (control).

It supports applications such as AI-equipped IP cameras, robot vision, and so on.

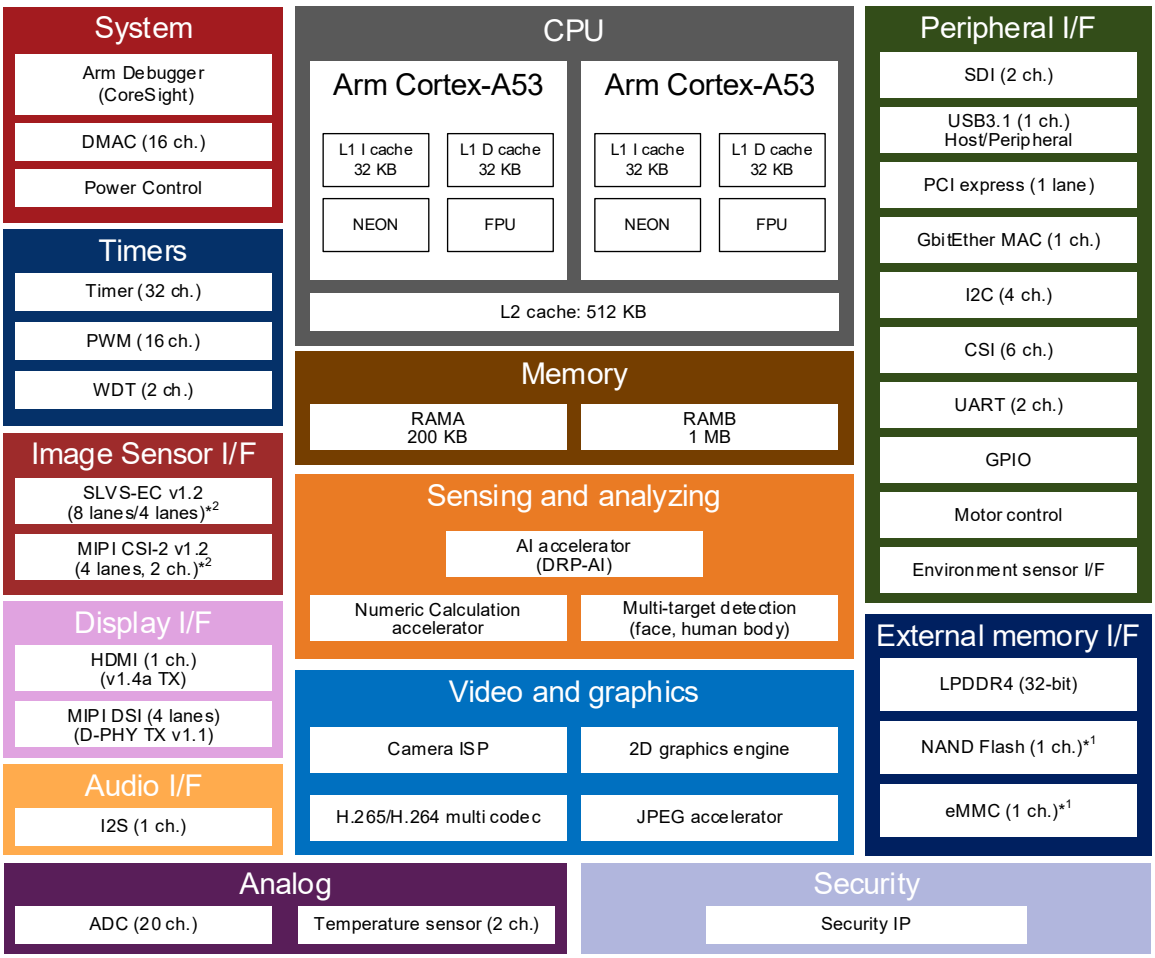
The main features are listed below.

■ High-speed ISP for use with cameras

This proprietary ISP supports SLVS-EC and MIPI-CSI as CMOS image sensor interfaces. It allows the capture of high-speed, high-resolution images such as high-resolution still images and 4K30p video.

■ AI accelerator

The dynamic reconfigurable processor (DRP) technology from Renesas supports various types of neural network and is capable of realizing embedded AI while featuring low power consumption.



Note 1. Only one of either NAND flash memory or eMMC can be used.

Note 2. The use of SLVS-EC and MIPI CSI-2 v1.2 are exclusive of each other.

Figure 1 Diagram of Functional Overview

1.2 Functions

Table 1 Overview of Functions (1/2)

Item	Function
CPU	• Cortex-A53 dual core: 996 MHz – L1 cache: 32 Kbytes (for instructions) + 32 Kbytes (for data) for each core – L2 cache: 512 Kbytes – FPU, Neon extension – ECC supported • Debugger interface (JTAG) – CoreSight debugging components incorporated – ETF (64-Kbyte trace RAM), ETR, and STM incorporated
Memory	• Work RAM A (RAMA): 200 Kbytes (with ECC) • Work RAM B (RAMB): 1 Mbyte • Boot ROM: 128 Kbytes
Timers	• Watchdog timer (WDT): 2 channels (CA53 core 0, CA53 core 1) • Compare-match timer: 32 channels • Pulse-width modulation timer (PWM): 16 channels • Internal real-time clock (RTC)
DMA controller	DMA (16 channels): Supports startup from the hardware (CSI, UART)
CMOS image sensor interfaces	• SLVS-EC v1.2 8 lanes x 1/4 lanes × 2 • MIPI CSI-2 v1.2 4 lanes × 2 • Formats: – RAW: 8/10/12 bits
Audio interfaces	I2S interface for connecting to the external audio codec
Sensing and analyzing	• AI accelerator (DRP-AI) • Multi-target detection IP (face, human body) • Numeric calculation accelerator
Video & graphics	• Camera ISP – 4K2K 30 fps / Full-HD 30 fps × 2 / VGA 800 fps / QVGA 1600 fps supported – HDR processing – 3D noise reduction • H.265/H.264 multi codec – H.265 encoding and decoding H.265/HEVC main profile at level 5 3840 × 2160 × 30 fps encoding, 3840 × 2160 × 30 fps decoding – H.264 encoding and decoding performance H.264/AVC baseline/main/high profile at level 5.1 1920 × 1080 p × 120 fps encoding, 1920 × 1080 p × 120 fps decoding • JPEG accelerator – JPEG extended DCT-based process/baseline-process compliant • 2D graphics engine • 200 Mpixels per second fill rate (200-MHz clock, single pipeline)

Table 1 Overview of Functions (2/2)

Item	Function
External memory interfaces	• LPDDR4 interface – 3200 Mbps – 32-bit data width • NAND flash interface – ONFI1.0 compliant – 4-/8-bit ECC • eMMC interface conforming to eMMC version 4.51 – Supports HS200 (high-speed DDR and HS400 are not supported) – 1/4/8-bit data bus
Peripheral interfaces	• SD host interface (SDI): 2 channels (SD specification version 3.01 compliant) – SD memory / I/O card interface – SD memory card access for SD, SDHC, and SDXC • USB interface: 1 channel – USB3.1 Gen1 standard compliant – Support for super-speed (5 Gbps), high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transfer (low-speed is only supported for the host controller) • PCI Express interface: Gen2 (5GT/s), 1 lanes – PCI express base specification revision 4.0 compliant • Gigabit Ethernet MAC interface: 1 channel – Supports interface conforming to IEEE802.3 PHY GMII, MII • I2C interface: 4 channels • 3-wire serial interface: 6 channels • UART: 2 channels • Motor control • Environment sensor interface • GPIO
Display interfaces	• HDMI Tx interface v1.4a: 1 channel – Up to 1080 p supported • MIPI DSI Tx interface v1.1, 4 lanes
Security engine	• Encryption and decryption algorithms • Hardware random number generator • AES, RSA, SHA
Analog	• ADC 20 channels (12 bits, 600 ksamples /sec) • Temperature sensor: 2 channels
Power control	• On-chip power-on/off, sequence control

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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